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Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	14742	sleep adj mode	US-PGPUB; USPAT; USOCR; EPO; JPO	OR	ON	2007/10/07 10:13
L2	79573	sram or (static adj ram) or (static adj random adj access adj memory)	US-PGPUB; USPAT; USOCR; EPO; JPO	OR	ON	2007/10/07 10:14
L3	1707	1 and 2	US-PGPUB; USPAT; USOCR; EPO; JPO	OR	ON	2007/10/07 10:14
L4	84996	"365"/$.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO	OR	ON	2007/10/07 10:14
L5	240	3 and 4	US-PGPUB; USPAT; USOCR; EPO; JPO	OR	ON	2007/10/07 10:14
L6	266	houston-theodore-w$.in.	US-PGPUB; USPAT; USOCR; EPO; JPO	OR	ON	2007/10/07 10:14

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Inventor Name Search Result

Your Search was:

Last Name = HOUSTON
First Name = THEODORE

Application#	Patent#	Status	Date Filed	Title	Inventor Name
09069569	6118161	150	04/29/1998	SELF-ALIGNED TRENCHED-CHANNEL LATERAL-CURRENT-FLOW TRANSISTOR	HOUSTON, THEODORE
60011988	Not Issued	159	02/21/1996	REDUCING NON-UNIFORMITY IN A REFILL LAYER THICKNESS FOR A SEMICONDUCTOR DEVICE	HOUSTON, THEODORE
60172058	Not Issued	159	12/23/1999	DYNAMIC THRESHOLD VOLTAGE 6T SRAM CELL	HOUSTON, THEODORE S.
60173042	Not Issued	159	12/23/1999	DYNAMIC THRESHOLD VOLTAGE 4T SRAM CELL	HOUSTON, THEODORE S.
09491942	6362117	150	01/26/2000	METHOD OF MAKING INTEGRATED CIRCUIT WITH CLOSELY SPACED COMPONENTS	HOUSTON, THEODORE W
60259400	Not Issued	159	12/30/2000	Means for forming sol	HOUSTON, THEODORE W
09428835	Not Issued	161	10/28/1999	LOCAL INTERCONNECT STRUCTURES AND METHODS	HOUSTON, THEODORE W
09589951	6207511	150	06/08/2000	Self-aligned trenched-channel lateral-current-flow transistor	HOUSTON, THEODORE W.
09661659	6376344	150	09/14/2000	SEMICONDUCTOR DEVICE WITH FULLY SELF-ALIGNED LOCAL INTERCONNECTS, AND METHOD FOR FABRICATING THE DEVICE	HOUSTON, THEODORE W.
09661735	6737347	150	09/14/2000	SEMICONDUCTOR DEVICE WITH FULLY SELF-ALIGNED LOCAL INTERCONNECTS, AND METHOD FOR FABRICATING THE DEVICE	HOUSTON, THEODORE W.

09685038	6512272	150	10/10/2000	INCREASED GATE TO BODY COUPLING AND APPLICATION TO DRAM AND DYNAMIC CIRCUITS	HOUSTON, THEODORE W.
09697922	6362058	150	10/26/2000	Method for controlling an implant profile in the channel of a transistor	HOUSTON, THEODORE W.
09727197	Not Issued	161	11/30/2000	METHOD FOR MANUFACTURING A HIGH-FREQUENCY INTEGRATED CIRCUIT FOR REDUCING CROSS-TALK AND FACILITATING ENERGY STORAGE	HOUSTON, THEODORE W.
09877534	6552923	150	06/08/2001	SRAM WITH WRITE-BACK ON READ	HOUSTON, THEODORE W.
09921168	6826730	150	08/02/2001	SYSTEM AND METHOD FOR CONTROLLING CURRENT IN AN INTEGRATED CIRCUIT	HOUSTON, THEODORE W.
09961213	6569741	150	09/21/2001	HYDROGEN ANNEAL BEFORE GATE OXIDATION	HOUSTON, THEODORE W.
09976983	6731533	150	10/12/2001	LOADLESS 4T SRAM CELL WITH PMOS DRIVERS	HOUSTON, THEODORE W.
09997120	6576519	150	11/28/2001	METHOD AND APPARATUS FOR FABRICATING SELF-ALIGNED CONTACTS IN AN INTEGRATED CIRCUIT	HOUSTON, THEODORE W.
09999030	6597610	150	10/25/2001	SYSTEM AND METHOD FOR PROVIDING STABILITY FOR A LOW POWER STATIC RANDOM ACCESS MEMORY CELL	HOUSTON, THEODORE W.
10001473	6635550	150	11/01/2001	SEMICONDUCTOR ON INSULATOR DEVICE ARCHITECTURE AND METHOD OF CONSTRUCTION	HOUSTON, THEODORE W.
10001707	7199471	150	10/25/2001	METHOD AND APPARATUS FOR REDUCING CAPACITIVE COUPLING BETWEEN LINES IN AN INTEGRATED CIRCUIT	HOUSTON, THEODORE W.
10005863	6461933	150	11/08/2001	SPIMOX/SIMOX COMBINATION WITH ITOX OPTION	HOUSTON, THEODORE W.
10007839	7101772	150	11/08/2001	MEANS FOR FORMING SOI	HOUSTON, THEODORE W.

10008690	6576957	150	11/08/2001	ETCH-STOPPED SOI BACK-GATE CONTACT	HOUSTON, THEODORE W.
10010653	6972448	150	11/08/2001	SUB-LITHOGRAPHICS OPENING FOR BACK CONTACT OR BACK GATE	HOUSTON, THEODORE W.
10028199	6687145	150	12/20/2001	STATIC RANDOM ACCESS MEMORY CELL AND METHOD	HOUSTON, THEODORE W.
10028484	Not Issued	168	12/20/2001	4T memory with boost of stored voltage between standby and active	HOUSTON, THEODORE W.
10029494	Not Issued	160	12/20/2001	Refresh at beginning of 4T active cycle	HOUSTON, THEODORE W.
10035923	6483739	150	12/31/2001	4T MEMORY WITH BOOST OF STORED VOLTAGE BETWEEN STANDBY AND ACTIVE	HOUSTON, THEODORE W.
10036095	Not Issued	161	12/31/2001	Partial trench body ties in sram cell	HOUSTON, THEODORE W.
10036296	6639826	150	12/31/2001	MEMORY CELL OPERATION USING RAMPED WORDLINES	HOUSTON, THEODORE W.
10036322	Not Issued	161	12/31/2001	Body-tied-to-source with partial trench	HOUSTON, THEODORE W.
10036324	6628540	150	12/31/2001	BIAS CELL FOR FOUR TRANSISTOR (4T) SRAM OPERATION	HOUSTON, THEODORE W.
10039124	6768144	150	12/31/2001	METHOD AND APPARATUS FOR REDUCING LEAKAGE CURRENT IN AN SRAM ARRAY	HOUSTON, THEODORE W.
10039810	6563158	150	11/16/2001	METHOD AND APPARATUS FOR VOLTAGE STIFFENING IN AN INTEGRATED CIRCUIT	HOUSTON, THEODORE W.
10054957	Not Issued	120	01/25/2002	Asymmetrical devices for short gate length performance with disposable sidewall	HOUSTON, THEODORE W.
10061540	Not Issued	161	10/25/2001	Stacked vias and method	HOUSTON, THEODORE W.
10085646	6750543	150	02/27/2002	SEMICONDUCTOR DEVICE WITH FULLY SELF-ALIGNED LOCAL INTERCONNECTS, AND METHOD FOR FABRICATING THE DEVICE	HOUSTON, THEODORE W.
10140418	Not Issued	161	05/06/2002	Selectively increased interlevel capacitance	HOUSTON, THEODORE W.
10142336	6703673	150	05/09/2002	SOI DRAM HAVING P-DOPED	HOUSTON,

				POLY GATE FOR A MEMORY PASS TRANSISTOR	THEODORE W.
10177773	6573549	150	06/21/2002	DYNAMIC THRESHOLD VOLTAGE 6T SRAM CELL	HOUSTON, THEODORE W.
10178063	Not Issued	160	06/21/2002	Dynamic threshold voltage 4T SRAM cell	HOUSTON, THEODORE W.
10180140	6710391	150	06/26/2002	INTEGRATED DRAM PROCESS/STRUCTURE USING CONTACT PILLARS	HOUSTON, THEODORE W.
10185380	6611451	150	06/28/2002	MEMORY ARRAY AND WORDLINE DRIVER SUPPLY VOLTAGE DIFFERENTIAL IN STANDBY	HOUSTON, THEODORE W.
10227615	6787469	150	08/23/2002	DOUBLE PATTERN AND ETCH OF POLY WITH HARD MASK	HOUSTON, THEODORE W.
10230830	6677190	150	08/29/2002	SELF-ALIGNED BODY CONTACT IN A SEMICONDUCTOR DEVICE	HOUSTON, THEODORE W.
10233352	6734521	150	08/30/2002	INTEGRATED CIRCUIT CELLS	HOUSTON, THEODORE W.
10320222	6735143	150	12/16/2002	SYSTEM FOR REDUCING POWER CONSUMPTION IN MEMORY DEVICES	HOUSTON, THEODORE W.
10324244	Not Issued	161	12/19/2002	Semiconductor apparatus having contacts of multiple heights and method of making same	HOUSTON, THEODORE W.
10337055	6791864	150	01/06/2003	COLUMN VOLTAGE CONTROL FOR WRITE	HOUSTON, THEODORE W.

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Application#	Patent#	Status	Date Filed	Title	Inventor Name
10337069	7027346	150	01/06/2003	BIT LINE CONTROL FOR LOW POWER IN STANDBY	HOUSTON, THEODORE W.
10349277	7039818	150	01/22/2003	LOW LEAKAGE SRAM SCHEME	HOUSTON, THEODORE W.
10400353	Not Issued	41	03/27/2003	Hydrogen anneal before gate oxidation	HOUSTON, THEODORE W.
10417581	6974968	150	04/17/2003	METHOD AND APPARATUS FOR FABRICATING SELF-ALIGNED CONTACTS IN AN INTEGRATED CIRCUIT	HOUSTON, THEODORE W.
10417627	Not Issued	41	04/17/2003	Method of Fabrication Etch-Stopped Soi Back-Gate Contact	HOUSTON, THEODORE W.
10616755	6925010	150	07/10/2003	STATIC RANDOM ACCESS MEMORY DEVICE HAVING DECREASED SENSITIVITY TO VARIATIONS IN CHANNEL PHYSICAL CHARACTERISTICS	HOUSTON, THEODORE W.
10618473	Not Issued	90	07/11/2003	SYSTEM FOR REDUCING ROW PERIPHERY POWER CONSUMPTION IN MEMORY DEVICES	HOUSTON, THEODORE W.
10628148	7148121	150	07/28/2003	SEMICONDUCTOR ON INSULATOR DEVICE ARCHITECTURE AND METHOD OF CONSTRUCTION	HOUSTON, THEODORE W.
10635185	7158402	150	08/06/2003	ASYMMETRIC STATIC RANDOM ACCESS MEMORY DEVICE HAVING REDUCED BIT LINE LEAKAGE	HOUSTON, THEODORE W.
10664547	Not Issued	66	09/19/2003	Integrated DRAM process/structure using contact	HOUSTON, THEODORE W.

				global variation	
10870355	Not Issued	164	06/17/2004	STAGGERED MEMORY CELL ARRAY	HOUSTON, THEODORE W.
10895512	Not Issued	90	07/20/2004	METHOD AND SYSTEM FOR CONTIGUOUS PROXIMITY CORRECTION FOR SEMICONDUCTOR MASKS	HOUSTON, THEODORE W.
10945725	7120082	150	09/21/2004	SYSTEM FOR REDUCING ROW PERIPHERY POWER CONSUMPTION IN MEMORY DEVICES	HOUSTON, THEODORE W.
10993815	7216310	150	11/19/2004	DESIGN METHOD AND SYSTEM FOR OPTIMUM PERFORMANCE IN INTEGRATED CIRCUITS THAT USE POWER MANAGEMENT	HOUSTON, THEODORE W.
11018602	7132340	150	12/21/2004	APPLICATION OF POST-PATTERN RESIST TRIM FOR REDUCING POCKET-SHADOWING IN SRAMS	HOUSTON, THEODORE W.
11109224	Not Issued	93	04/18/2005	BIT LINE CONTROL FOR LOW POWER IN STANDBY	HOUSTON, THEODORE W.
11143038	Not Issued	71	06/02/2005	Static random-access memory having reduced bit line precharge voltage and method of operating the same	HOUSTON, THEODORE W.
11171033	7236396	150	06/30/2005	AREA EFFICIENT IMPLEMENTATION OF SMALL BLOCKS IN AN SRAM ARRAY	HOUSTON, THEODORE W.
11191349	Not Issued	95	07/28/2005	MEMORY ARRAY WITH A DELAYED WORDLINE BOOST	HOUSTON, THEODORE W.
11191741	7164596	150	07/28/2005	SRAM CELL WITH COLUMN SELECT LINE	HOUSTON, THEODORE W.
11202141	Not Issued	41	08/11/2005	SRAM cell using separate read and write circuitry	HOUSTON, THEODORE W.
11204064	Not Issued	41	08/15/2005	Static random access memory device having a voltage-controlled word line driver for retain till accessed mode and method of operating the same	HOUSTON, THEODORE W.
11234346	Not Issued	120	09/23/2005	Write assist for latch and memory circuits	HOUSTON, THEODORE W.
11234910	Not	41	09/26/2005	Thermostatic biasing controller,	HOUSTON,

	Issued			method of thermostatic biasing and an integrated circuit employing the same	THEODORE W.
11237082	Not Issued	61	09/28/2005	Static random access memory device having bit line voltage control for retain till accessed mode and method of operating the same	HOUSTON, THEODORE W.
11238932	Not Issued	30	09/29/2005	SRAM cell with asymmetrical pass gate	HOUSTON, THEODORE W.
11239626	Not Issued	30	09/29/2005	SRAM cell with asymmetrical transistors for reduced leakage	HOUSTON, THEODORE W.
11239834	Not Issued	41	09/30/2005	Sub-lithographics opening for back contact or back gate	HOUSTON, THEODORE W.
11259999	Not Issued	41	10/27/2005	Body bias coordinator, method of coordinating a body bias and sub-circuit power supply employing the same	HOUSTON, THEODORE W.
11268974	Not Issued	41	11/08/2005	Method for testing transistors having an active region that is common with other transistors and a testing circuit for accomplishing the same	HOUSTON, THEODORE W.
11553903	Not Issued	30	10/27/2006	INTEGRATED VIRTUAL VOLTAGE CIRCUIT	HOUSTON, THEODORE W.
11609678	Not Issued	25	12/12/2006	TUNABLE VOLTAGE CONTROLLER FOR A SUB-CIRCUIT AND METHOD OF OPERATING THE SAME	HOUSTON, THEODORE W.
11624355	Not Issued	30	01/18/2007	TEMPERATURE DEPENDENT BACK-BIAS FOR A MEMORY ARRAY	HOUSTON, THEODORE W.
11781392	Not Issued	17	07/23/2007	ADAPTIVE VOLTAGE CONTROL FOR SRAM	HOUSTON, THEODORE W.
11828465	Not Issued	17	07/26/2007	MEMORY ARRAY WITH A DELAYED WORDLINE BOOST	HOUSTON, THEODORE W.
11828476	Not Issued	17	07/26/2007	MEMORY ARRAY WITH A DELAYED WORDLINE BOOST	HOUSTON, THEODORE W.

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				pillars	
10666336	6800523	150	09/17/2003	INTEGRATED DRAM PROCESS/STRUCTURE USING CONTACT PILLARS	HOUSTON, THEODORE W.
10667615	Not Issued	41	09/22/2003	Multi-gate one-transistor dynamic random access memory	HOUSTON, THEODORE W.
10682729	6873008	150	10/10/2003	ASYMMETRICAL DEVICES FOR SHORT GATE LENGTH PERFORMANCE WITH DISPOSABLE SIDEWALL	HOUSTON, THEODORE W.
10691410	6954918	150	10/22/2003	INTEGRATED CIRCUIT CELLS	HOUSTON, THEODORE W.
10691426	6996787	150	10/22/2003	INTEGRATED CIRCUIT CELLS	HOUSTON, THEODORE W.
10701669	6925025	150	11/05/2003	SRAM DEVICE AND A METHOD OF POWERING-DOWN THE SAME	HOUSTON, THEODORE W.
10704858	6900656	150	11/10/2003	METHOD OF TESTING AN INTEGRATED CIRCUIT AND AN INTEGRATED CIRCUIT TEST APPARATUS	HOUSTON, THEODORE W.
10732970	Not Issued	121	12/11/2003	SRAM device and a method of operating the same to reduce leakage current during a sleep mode	HOUSTON, THEODORE W.
10733038	Not Issued	71	12/11/2003	Static random access memory device having reduced leakage current during active mode and a method of operating thereof	HOUSTON, THEODORE W.
10733485	6922370	150	12/11/2003	HIGH PERFORMANCE SRAM DEVICE AND METHOD OF POWERING-DOWN THE SAME	HOUSTON, THEODORE W.
10745429	6982915	150	12/22/2003	SRAM WITH TEMPERATURE-DEPENDENT VOLTAGE CONTROL IN SLEEP MODE	HOUSTON, THEODORE W.
10818799	Not Issued	161	04/05/2004	Semiconductor device with fully self-aligned local interconnects, and method for fabricating the device	HOUSTON, THEODORE W.
10857420	Not Issued	161	05/27/2004	Semiconductor apparatus having contacts of multiple heights and method of making same	HOUSTON, THEODORE W.
10862637	Not Issued	40	06/07/2004	Statistical evaluation of circuit robustness separating local and	HOUSTON, THEODORE W.

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Application#	Patent#	Status	Date Filed	Title	Inventor Name
11848442	Not Issued	17	08/31/2007	SRAM BIAS FOR READ AND WRITE	HOUSTON, THEODORE W.
60211259	Not Issued	159	06/13/2000	Sram with write-back on read	HOUSTON, THEODORE W.
60235096	Not Issued	159	09/25/2000	Hydrogen anneal before gate oxidation	HOUSTON, THEODORE W.
60244726	Not Issued	159	10/31/2000	Loadless 4T SRAM cell with PMOS drivers	HOUSTON, THEODORE W.
60257326	Not Issued	159	12/20/2000	Semiconductor on insulator device architecture and method of construction	HOUSTON, THEODORE W.
60257726	Not Issued	159	12/21/2000	Method and apparatus for reducing capacitive coupling between lines in an integrated circuit	HOUSTON, THEODORE W.
60258768	Not Issued	159	12/29/2000	Improved static random access memory cell and method	HOUSTON, THEODORE W.
60258819	Not Issued	159	12/29/2000	System and method for providing stability for a static random access memory cell	HOUSTON, THEODORE W.
60258879	Not Issued	159	12/29/2000	Stacked vias and method	HOUSTON, THEODORE W.
60259276	Not Issued	159	12/31/2000	4T memory with boost of stored voltage between standby and active	HOUSTON, THEODORE W.
60259277	Not Issued	159	12/31/2000	Etch-stopped SOI back-gate contact	HOUSTON, THEODORE W.
60259299	Not Issued	159	12/31/2000	Bias cell for four transistor (4T) sram operation	HOUSTON, THEODORE W.
60259300	Not Issued	159	12/31/2000	Partial trench body ties in sram cell	HOUSTON, THEODORE W.
60259301	Not	159	12/31/2000	Sub-lithographics opening for	HOUSTON,

	Issued			back contact or back gate	THEODORE W.
60259311	Not Issued	159	12/31/2000	Body-tie-to-source (BTS) with partial trench	HOUSTON, THEODORE W.
60259312	Not Issued	159	12/31/2000	Refresh at beginning of 4T active cycle	HOUSTON, THEODORE W.
60259320	Not Issued	159	12/31/2000	Back-gate contact as SOI moat edge	HOUSTON, THEODORE W.
60299907	Not Issued	159	06/21/2001	Etch-stopping SOI structure	HOUSTON, THEODORE W.
60299966	Not Issued	159	06/21/2001	Sub-lithographics opening for back contact or back gate	HOUSTON, THEODORE W.
60344521	Not Issued	159	12/28/2001	Memory with supply voltage controlled by row	HOUSTON, THEODORE W.
60344631	Not Issued	159	12/28/2001	Double pattern and etch of poly with hard mask	HOUSTON, THEODORE W.
60353434	Not Issued	159	01/31/2002	Semiconductor apparatus having contacts of multiple heights and method of making same	HOUSTON, THEODORE W.
60534723	Not Issued	159	01/07/2004	Transistor design methodology for optimum performance in integrated circuits that use power management	HOUSTON, THEODORE W.
06070380	Not Issued	161	08/27/1979	MESFET SEMICONDUCTOR DEVICE AND METHOD OF MAKING	HOUSTON, THEODORE W.
06070382	Not Issued	161	08/27/1979	MESFET SEMICONDUCTOR DEVICE AND METHOD OF MAKING	HOUSTON, THEODORE W.
06324180	4490632	150	11/23/1981	NONINVERTING AMPLIFIER CIRCUIT FOR ONE PROPAGATION DELAY COMPLEX LOGIC GATES	HOUSTON, THEODORE W.
06334405	4455738	150	12/24/1981	SELF-ALIGNED GATE METHOD FOR MAKING MESFET SEMICONDUCTOR	HOUSTON, THEODORE W.
06334948	4466174	150	12/28/1981	METHOD FOR FABRICATING MESFET DEVICE USING A DOUBLE LOCOS PROCESS	HOUSTON, THEODORE W.
06339542	Not Issued	167	01/15/1982	METHOD OFMAKING A MESFET DEVICE	HOUSTON, THEODORE W.
06339543	4481704	150	01/15/1982	METHOD OF MAKING AN IMPROVED MESFET SEMICONDUCTOR DEVICE	HOUSTON, THEODORE W.
06363194	4484310	150	03/29/1982	STATIC NONINVERTING	HOUSTON,

				MEMORY CELL FOR ONE PROPAGATION DELAY MEMORY CIRCUITS	THEODORE W.
06557800	Not Issued	163	12/05/1983	ASYMMETRICAL SI MESFET DEVICE STRUCTURE WITH REDUCED SOURCE RESISTANCE AND REDUCED SATURATION CONDUCTANCE	HOUSTON, THEODORE W.
06570109	Not Issued	167	01/12/1984	METHOD OF MAKING A MESFET DEVICE	HOUSTON, THEODORE W.
06588630	4553316	150	03/12/1984	SELF-ALIGNED GATE METHOD FOR MAKING MESFET SEMICONDUCTOR	HOUSTON, THEODORE W.
06646871	4620297	150	08/31/1984	SCHMITT TRIGGER BASED MEMORY CELL WITH ASSISTED TURN ON	HOUSTON, THEODORE W.
06743350	Not Issued	161	06/11/1985	COMPRESSED ACCESS TIME RANDOM ACCESS MEMORY	HOUSTON, THEODORE W.
06879654	Not Issued	166	06/27/1986	CROSS-COUPLED COMPLEMENTARY BIT LINES FOR A SEMICONDUCTOR MEMORY	HOUSTON, THEODORE W.
06903330	Not Issued	166	09/03/1986	COMPOUND DOMINO CMOS CIRCUIT	HOUSTON, THEODORE W.
07043381	4811301	150	04/28/1987	LOW-POWER, NOISE-RESISTANT READ-ONLY MEMORY	HOUSTON, THEODORE W.
07081419	4870598	150	08/04/1987	COMPREHENSIVE LOGIC CIRCUIT LAYOUT SYSTEM	HOUSTON, THEODORE W.
07100669	Not Issued	161	09/24/1987	COMPREHENSIVE LOGIC CIRCUIT LAYOUT SYSTEM	HOUSTON, THEODORE W.
07130769	4916336	150	12/09/1987	COLUMN SELECT CIRCUIT	HOUSTON, THEODORE W.
07211619	4953130	150	06/27/1988	MEMORY CIRCUIT WITH EXTENDED VALID DATA OUTPUT TIME	HOUSTON, THEODORE W.
07213814	Not Issued	166	06/30/1988	MEMORY DEVICE WITH END-OF CYCLE PRECHARGE	HOUSTON, THEODORE W.
07241516	5204990	150	09/07/1988	MEMORY CELL WITH CAPACITANCE FOR SINGLE EVENT UPSET PROTECTION	HOUSTON, THEODORE W.
07241524	4914629	150	09/07/1988	MEMORY CELL INCLUDING	HOUSTON,

				SINGLE EVENT UPSET RATE REDUCTION CIRCUITRY	THEODORE W.
07241681	4912675	150	09/07/1988	SINGLE EVENT UPSET HARDENED MEMORY CELL	HOUSTON, THEODORE W.
07252200	4956814	150	09/30/1988	MEMORY CELL WITH IMPROVED SINGLE EVENT UPSET RATE REDUCTION CIRCUITRY	HOUSTON, THEODORE W.
07252287	4932002	150	09/30/1988	BIT LINE LATCH SENSE AMP	HOUSTON, THEODORE W.
07252291	4956815	150	09/30/1988	MEMORY CELL WITH INCREASED STABILITY	HOUSTON, THEODORE W.

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Application#	Patent#	Status	Date Filed	Title	Inventor Name
07270168	4899315	150	11/14/1988	LOW-POWER, NOISE-RESISTANT READ-ONLY MEMORY	HOUSTON, THEODORE W.
07285440	5053848	150	12/16/1988	APPARATUS FOR PROVIDING SINGLE EVENT UPSET RESISTANCE FOR SEMICON-DUCTOR DEVICES	HOUSTON, THEODORE W.
07287338	5018102	150	12/20/1988	MEMORY HAVING SELECTED STATE ON POWER-UP	HOUSTON, THEODORE W.
07288399	Not Issued	161	12/22/1988	CONTROL OF SENSE AMP LATCH TIMING	HOUSTON, THEODORE W.
07288505	4985865	150	12/21/1988	ASYMMETRICAL DELAY FOR CONTROLLING WORD LINE SELECTION	HOUSTON, THEODORE W.
07288532	Not Issued	163	12/21/1988	USE OF ASYMMETRICAL DELAY CIRCUITRY FOR GLITCH PROTECTION	HOUSTON, THEODORE W.
07288541	Not Issued	166	12/21/1988	SEU HARDENED MEMORY CELL	HOUSTON, THEODORE W.
07288544	Not Issued	166	12/21/1988	BIT LINE PRECHARGE/EQUALIZATION TIMING RELATIVE TO WORD LINE TIMING FOR NOISE IMMUNITY	HOUSTON, THEODORE W.
07291724	Not Issued	166	12/29/1988	MEMORY CELL WITH GUARD REGION FOR REDUCING SOFT ERROR RATE	HOUSTON, THEODORE W.
07302842	5084873	150	01/27/1989	CHIP ERROR DETECTOR	HOUSTON, THEODORE W.
07314619	5023874	150	02/23/1989	SCREENING LOGIC CIRCUITS FOR PREFERRED STATES	HOUSTON, THEODORE W.
07315364	Not Issued	163	02/23/1989	SEGMENTED BIT LINE SRAM ARCHITECTURE	HOUSTON, THEODORE W.

07336957	Not Issued	161	05/18/1989	COMPREHENSIVE LOGIC CIRCUIT LAYOUT SYSTEM	HOUSTON, THEODORE W.
07358298	Not Issued	166	05/26/1989	MULTIPLE INPUT BUFFERS FOR ADDRESS BITS	HOUSTON, THEODORE W.
07365390	5160989	150	06/13/1989	EXTENDED BODY CONTACT FOR SEMICONDUCTOR OVER INSULATOR TRANSISTOR	HOUSTON, THEODORE W.
07375097	Not Issued	166	06/30/1989	MULTIPLE COMPOUND DOMINO LOGIC CIRCUIT	HOUSTON, THEODORE W.
07395853	Not Issued	166	08/18/1989	ON CHIP ERROR DETECTION CIRCUIT	HOUSTON, THEODORE W.
07411087	Not Issued	166	09/22/1989	MEMORY WITH SELECTIVE ADDRESS TRANSITION DETECTION FOR CACHE OPERATION	HOUSTON, THEODORE W.
07488331	Not Issued	166	03/02/1990	SOI SRAM LAYOUT FOR LOW RESISTANCE GATE	HOUSTON, THEODORE W.
07499128	4975597	150	03/26/1990	COLUMN SELECT CIRCUIT	HOUSTON, THEODORE W.
07502393	5107139	150	03/30/1990	ON-CHIP TRANSIENT EVENT DETECTOR	HOUSTON, THEODORE W.
07521000	4980860	150	05/08/1990	CROSS-COUPLED COMPLEMENTARY BIT LINES FOR A SEMICONDUCTOR MEMORY WITH PULL-UP CIRCUITRY	HOUSTON, THEODORE W.
07542666	5015882	150	06/25/1990	COMPOUND DOMINO CMOS CIRCUIT	HOUSTON, THEODORE W.
07546080	5150309	150	06/29/1990	COMPREHENSIVE LOGIC CIRCUIT LAYOUT SYSTEM	HOUSTON, THEODORE W.
07546612	5119313	150	06/29/1990	COMPREHENSIVE LOGIC CIRCUIT LAYOUT SYSTEM	HOUSTON, THEODORE W.
07561473	Not Issued	163	08/01/1990	MEMORY CELL WITH GUARD REGION FOR REDUCING SOFT ERROR RATE	HOUSTON, THEODORE W.
07563722	5046044	150	08/01/1990	SEU HARDENED MEMORY CELL	HOUSTON, THEODORE W.
07573598	5210715	150	08/27/1990	MEMORY CIRCUIT WITH EXTENDED VALID DATA OUTPUT TIME	HOUSTON, THEODORE W.
07596631	Not Issued	163	10/11/1990	BITLINE PRECHARGE/EQUALIZATION TIMING RELATIVE TO WORDLINE TIMING FOR NOISE IMMUNITY	HOUSTON, THEODORE W.

07627562	5208489	150	12/10/1990	MULTIPLE COMPOUND DOMINO LOGIC CIRCUIT	HOUSTON, THEODORE W.
07628933	5095348	150	12/13/1990	SEMICONDUCTOR ON INSULATOR TRANSISTOR	HOUSTON, THEODORE W.
07647111	5185280	150	01/29/1991	METHOD OF FABRICATING A SOI TRANSISTOR WITH POCKET IMPLANT AND BODY- TO-SOURCE (BTS) CONTACT	HOUSTON, THEODORE W.
07647615	5193076	150	01/28/1991	CONTROL OF SENSE AMPLIFIER LATCH TIMING	HOUSTON, THEODORE W.
07683116	Not Issued	166	04/08/1991	MEMORY DEVICE WITH END-OF-CYCLE PRECHARGE	HOUSTON, THEODORE W.
07706621	5313422	150	05/29/1991	DIGITALLY CONTROLLED DELAY APPLIED TO ADDRESS DECODER FOR WRITE VS. READ	HOUSTON, THEODORE W.
07707517	5198710	150	05/30/1991	BI-DIRECTIONAL DIGITAL NOISE GLITCH FILTER	HOUSTON, THEODORE W.
07708117	5079604	150	05/29/1991	SOI LAYOUT FOR LOW RESISTANCE GATE	HOUSTON, THEODORE W.
07719430	5206533	150	06/24/1991	TRANSISTOR DEVICE WITH RESISTIVE COUPLING	HOUSTON, THEODORE W.
07719900	.Not Issued	166	06/24/1991	SINGLE EVENT UPSET HARDENED MEMORY CELL	HOUSTON, THEODORE W.
07737584	5157335	150	07/25/1991	ON-CHIP ERROR DETECTION CIRCUIT	HOUSTON, THEODORE W.
07754281	5214610	150	08/30/1991	MEMORY WITH SELECTIVE ADDRESS TRANSISTION DETECITON FOR CACHE OPERATION	HOUSTON, THEODORE W.
07807006	Not Issued	166	12/13/1991	DELAY COMPENSATION CIRCUIT	HOUSTON, THEODORE W.
07825743	Not Issued	166	01/23/1992	MULTIPLE INPUT BUFFERS FOR ADDRESS BITS	HOUSTON, THEODORE W.
07830214	Not Issued	166	01/30/1992	MEMORY DEVICE WITH END-OF-CYCLE PRECHARGE	HOUSTON, THEODORE W.
07837200	Not Issued	166	02/14/1992	TEMPERATURE COMPENSATION CIRCUIT AND METHOD OF OPERATION	HOUSTON, THEODORE W.
07842672	Not Issued	166	02/27/1992	METHOD AND SYSTEM FOR SCREENING LOGIC CIRCUITS	HOUSTON, THEODORE W.
07845302	5461577	150	03/03/1992	COMPREHENSIVE LOGIC CIRCUIT LAYOUT SYSTEM	HOUSTON, THEODORE W.
07901743	5361033	150	06/22/1992	ON CHIP BI-STABLE POWER-	HOUSTON,

				SPIKE DETECTION CIRCUIT	THEODORE W.
07909874	5325054	150	07/07/1992	METHOD AND SYSTEM FOR SCREENING RELIABILITY OF SEMICONDUCTOR CIRCUITS	HOUSTON, THEODORE W.
07919680	5215931	150	07/27/1992	METHOD OF MAKING EXTENDED BODY CONTACT FOR SEMICONDUCTOR OVER INSULATOR TRANSISTOR	HOUSTON, THEODORE W.

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Application#	Patent#	Status	Date Filed	Title	Inventor Name
07926263	Not Issued	161	08/06/1992	SOI TRANSISTOR WITH POCKET IMPLANT	HOUSTON, THEODORE W.
07972671	5310694	150	11/06/1992	METHOD FOR FORMING A TRANSISTOR DEVICE WITH RESISTIVE COUPLING	HOUSTON, THEODORE W.
07993502	5600274	150	12/17/1992	CIRCUIT AND METHOD FOR COMPENSATING VARIATIONS IN DELAY	HOUSTON, THEODORE W.
08000753	5436173	150	01/04/1993	METHOD FOR FORMING A SEMICONDUCTOR ON INSULATOR DEVICE	HOUSTON, THEODORE W.
08015874	Not Issued	166	02/03/1993	MULTIPLE INPUT BUFFERS FOR ADDRESS BITS	HOUSTON, THEODORE W.
08049045	Not Issued	166	04/16/1993	MEMORY CELL WITH CAPACITANCE FOR SINGLE EVENT UPSET PROTECTION	HOUSTON, THEODORE W.
08066698	Not Issued	166	05/25/1993	POWER REDUCTION IN A TEMPERATURE COMPENSATING TRANSISTOR CIRCUIT	HOUSTON, THEODORE W.
08084680	5406144	150	09/07/1993	POWER REDUCTION IN A TEMPERATURE COMPENSATING TRANSISTOR CIRCUIT	HOUSTON, THEODORE W.
08101348	5905290	150	08/02/1993	SINGLE EVENT UPSET HARDENED MEMORY CELL	HOUSTON, THEODORE W.
08117262	5396110	150	09/03/1993	PULSE GENERATOR CIRCUIT AND METHOD	HOUSTON, THEODORE W.
08131103	5404327	150	10/04/1993	MEMORY DEVICE WITH END OF CYCLE PRECHARGE UTILIZING WRITE SIGNAL AND DATA TRANSITION DETECTORS	HOUSTON, THEODORE W.

08150927	Not Issued	166	11/12/1993	SELECTIVE CURRENT LIMITS IN SEMICONDUCTOR DEVICES	HOUSTON, THEODORE W.
08165278	5438548	150	12/10/1993	SYNCHRONOUS MEMORY WITH REDUCED POWER ACCESS MODE	HOUSTON, THEODORE W.
08184746	5376846	150	01/21/1994	TEMPERATURE COMPENSATION CIRCUIT AND METHOD OF OPERATION	HOUSTON, THEODORE W.
08186215	Not Issued	166	01/24/1994	MULTIPLE INPUT BUFFERS FOR ADDRESS BITS	HOUSTON, THEODORE W.
08213789	Not Issued	166	03/16/1994	EFFICIENT CONTROL OF THE BODY VOLTAGE OF A FIELD EFFECT TRANSISTOR	HOUSTON, THEODORE W.
08219609	5544101	150	03/28/1994	MEMORY DEVICE HAVING A LATCHING MULTIPLEXER AND A MULTIPLEXER BLOCK THEREFOR	HOUSTON, THEODORE W.
08224226	5521524	150	04/07/1994	METHOD AND SYSTEM FOR SCREENING RELIABILITY OF SEMICONDUCTOR CIRCUITS	HOUSTON, THEODORE W.
08235753	Not Issued	161	04/29/1994	APPARATUS AND METHOD FOR CONVERTING VIDEO SIGNALS INTO VIDEO DISPLAY SEGMENTS OF A COMBINED VIDEO SIGNAL	HOUSTON, THEODORE W.
08236750	Not Issued	161	04/29/1994	DEVICE AND METHOD FOR CONVERTING DISPLAY SEGMENTS OF A COMBINED VIDEO SIGNAL INTO DISPLAY FIELDS OF MULTIPLE VIDEO SIGNALS	HOUSTON, THEODORE W.
08258135	Not Issued	161	06/10/1994	MEMORY CELL WITH CAPACITANCE FOR SINGLE EVENT UPSET PROTECTION	HOUSTON, THEODORE W.
08285244	5477151	150	08/03/1994	CAPACITOR AND DIODE CIRCUITRY FOR ON CHIP POWER SPIKE DETECTION	HOUSTON, THEODORE W.
08285457	5469065	150	08/03/1994	ON CHIP CAPACITOR BASED POWER SPIKE DETECTION	HOUSTON, THEODORE W.
08300503	5457695	150	09/02/1994	METHOD AND SYSTEM FOR SCREENING LOGIC CIRCUITS	HOUSTON, THEODORE W.
08300574	5422852	150	09/02/1994	METHOD AND SYSTEM FOR	HOUSTON,

				SCREENING LOGIC CIRCUITS	THEODORE W.
08321631	Not Issued	166	10/11/1994	VOLTAGE TRACKING DELAY CIRCUIT	HOUSTON, THEODORE W.
08352262	Not Issued	161	12/08/1994	SEMICONDUCTOR ON INSULATOR DEVICE AND A METHOD FOR FORMING A SEMICONDUCTOR ON INSULATOR DEVICE	HOUSTON, THEODORE W.
08368568	5615162	150	01/04/1995	SELECTIVE POWER TO MEMORY	HOUSTON, THEODORE W.
08368682	Not Issued	166	01/04/1995	SELECTABLE LOW POWER STATE IN SEMICONDUCTOR CIRCUITS	HOUSTON, THEODORE W.
08369951	5541882	150	01/09/1995	METHOD OF PERFORMING A COLUMN DECODE IN A MEMORY DEVICE AND APPARATUS THEREOF	HOUSTON, THEODORE W.
08371040	6069814	150	01/10/1995	MULTIPLE INPUT BUFFERS FOR ADDRESS BITS	HOUSTON, THEODORE W.
08376465	5498882	150	01/20/1995	EFFICIENT CONTROL OF THE BODY VOLTAGE OF A FIELD EFFECT TRANSISTOR	HOUSTON, THEODORE W.
08412429	5795810	150	03/29/1995	DEEP MESA ISOLATION IN SOI	HOUSTON, THEODORE W.
08431394	Not Issued	166	04/28/1995	SELECTIVE CURRENT LIMITS IN SEMICONDUCTOR DEVICES	HOUSTON, THEODORE W.
08434257	5917212	150	05/03/1995	MEMORY CELL WITH CAPACITANCE FOR SINGLE EVENT UPSET PROTECTION	HOUSTON, THEODORE W.
08472374	Not Issued	161	06/07/1995	ON CHIP ERROR DETECTION CIRCUIT	HOUSTON, THEODORE W.
08473690	Not Issued	161	06/07/1995	INTERACTIVE RECEIPT CARD WITH READ/WRITE MEMORY	HOUSTON, THEODORE W.
08476244	5565799	150	06/07/1995	ON CHIP ERROR DETECTION CIRCUIT	HOUSTON, THEODORE W.
08476245	Not Issued	161	06/07/1995	MEMORY CELL WITH CAPACITANCE FOR SINGLE EVENT UPSET PROTECTION	HOUSTON, THEODORE W.
08479741	Not Issued	162	06/07/1995	CONNECTION OF HIGH GOING AND LOW GOING TRANSITIONS	HOUSTON, THEODORE W.
08481972	6459910	150	06/07/1995	USE OF SPEECH	HOUSTON,

				RECOGNITION IN PAGER AND MOBILE TELEPHONE APPLICATIONS	THEODORE W.
08482067	5617038	150	06/07/1995	METHOD AND SYSTEM FOR SCREENING RELIABILITY OF SEMICONDUCTOR CIRCUITS	HOUSTON, THEODORE W.
08483424	Not Issued	161	06/07/1995	CHIP ERROR DETECTION CIRCUIT	HOUSTON, THEODORE W.
08483425	Not Issued	161	06/07/1995	CHIP ERROR DETECTION CIRCUIT	HOUSTON, THEODORE W.
08570368	5596286	150	12/11/1995	CURRENT LIMITING DEVICES TO REDUCE LEAKAGE, PHOTO, OR STAND-BY CURRENT IN AN INTEGRATED CIRCUIT	HOUSTON, THEODORE W.
08603564	Not Issued	166	02/21/1996	VOLTAGE TRACKING DELAY CIRCUIT	HOUSTON, THEODORE W.
08615576	5703517	150	03/12/1996	POWER REDUCTION IN A TEMPERATURE COMPENSATING TRANSISTOR CIRCUIT	HOUSTON, THEODORE W.
08695495	6121658	150	08/12/1996	DEEP MESA ISOLATION	HOUSTON, THEODORE W.
08701209	Not Issued	161	08/21/1996	CONNECTION OF HIGH GOING AND LOW GOING TRANSITIONS	HOUSTON, THEODORE W.
08743330	Not Issued	161	11/04/1996	SELECTABLE LOW POWER STATE IN SEMICONDUCTOR CIRCUITS	HOUSTON, THEODORE W.

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Application#	Patent#	Status	Date Filed	Title	Inventor Name
08761262	6477312	150	12/06/1996	INSTANT REPLAY SYSTEM	HOUSTON, THEODORE W.
08784434	Not Issued	161	01/16/1997	SELECTIVLEY LIMITING CURRENT IN AN INTEGRATED CIRCUIT	HOUSTON, THEODORE W.
08784793	Not Issued	161	01/16/1997	OPTIMIZING THE OPERATING CHARACTERISTICS OF A CMOS INTEGRATED CIRCUIT	HOUSTON, THEODORE W.
08804484	5909628	150	02/21/1997	REDUCING NON-UNIFORMITY IN A REFILL LAYER THICKNESS FOR A SEMICONDUCTOR DEVICE	HOUSTON, THEODORE W.
08813524	5936278	150	03/07/1997	SEMICONDUCTOR ON SILICON (SOI) TRANSISTOR WITH A HALO IMPLANT	HOUSTON, THEODORE W.
08825789	5917365	150	04/08/1997	OPTIMIZING THE OPERATING CHARACTERISTICS OF A CMOS INTEGRATED CIRCUIT	HOUSTON, THEODORE W.
08852982	6114945	150	05/08/1997	APPARATUS AND METHOD FOR PROOGRAMMABLE FAST COMPARTION OF A RESULT OF A LOGIC OPERATION WITH AN SELECTED RESULT	HOUSTON, THEODORE W.
08862449	6424016	150	05/23/1997	SOI DRAM HAVING P-DOPED POLYSILICON GATE FOR A MEMORY PASS TRANSISTOR	HOUSTON, THEODORE W.
08882467	Not Issued	163	06/25/1997	VOLTAGE TRACKING DELAY CIRCUIT	HOUSTON, THEODORE W.

08948901	Not Issued	161	10/10/1997	ADAPTIVELY RECONFIGURABLE INTEGRATED CIRCUIT AND METHOD THEREFOR	HOUSTON, THEODORE W.
08985697	6045625	150	12/05/1997	BURIED OXIDE WITH A THERMAL EXPANSION MATCHING LAYER FOR SOI	HOUSTON, THEODORE W.
08998153	5943258	150	12/24/1997	MEMORY WITH STORAGE CELLS HAVING SOI DRIVE AND ACCESS TRANSISTORS WITH TIED FLOATING BODY CONNECTIONS	HOUSTON, THEODORE W.
08998337	6037808	150	12/24/1997	DIFFERENTIAL SOI AMPLIFIERS HAVING TIED FLOATING BODY CONNECTIONS	HOUSTON, THEODORE W.
09046147	Not Issued	169	03/23/1998	SELECTABLE LOW POWER STATE IN SEMICONDUCTOR CIRCUITS	HOUSTON, THEODORE W.
09070213	6096612	150	04/30/1998	INCREASED EFFECTIVE TRANSISTOR WIDTH USING DOUBLE SIDEWALL SPACERS	HOUSTON, THEODORE W.
09092973	5942781	150	06/08/1998	TUNABLE THRESHOLD SOI DEVICE USING BACK GATE WELL	HOUSTON, THEODORE W.
09098188	6225175	150	06/16/1998	PROCESS FOR DEFINING ULTRA-THIN GEOMETRIES	HOUSTON, THEODORE W.
09106809	Not Issued	163	06/29/1998	STRUCTURE AND METHOD FOR A SELF-ALIGNED BACK GATE IN A SEMICONDUCTOR COMPONENT	HOUSTON, THEODORE W.
09140267	6043535	150	08/26/1998	SELF-ALIGNED IMPLANT UNDER TRANSISTOR GATE	HOUSTON, THEODORE W.
09161903	6061267	150	09/28/1998	MEMORY CIRCUITS, SYSTEMS, AND METHODS WITH CELLS USING BACK BIAS TO CONTROL THE THRESHOLD VOLTAGE OF ONE OR MORE CORRESONDING CELL TRANSISTORS	HOUSTON, THEODORE W.
09162865	6255853	150	09/29/1998	INTEGRATED CIRCUIT HAVING DYNAMIC LOGIC WITH REDUCED STANDBY LEAKAGE CURRENT	HOUSTON, THEODORE W.

09162866	6255854	150	09/29/1998	FEEDBACK STAGE FOR PROTECTING A DYNAMIC NODE IN AN INTEGRATED CIRCUIT HAVING DYNAMIC LOGIC	HOUSTON, THEODORE W.
09163267	6429684	150	09/29/1998	CIRCUIT HAVING DYNAMIC THRESHOLD VOLTAGE	HOUSTON, THEODORE W.
09211654	6308312	150	12/15/1998	SYSTEM AND METHOD FOR CONTROLLING LEAKAGE CURRENT IN AN INTEGRATED CIRCUIT USING CURRENT LIMITING DEVICES	HOUSTON, THEODORE W.
09211947	Not Issued	161	12/15/1998	SYSTEM AND METHOD FOR CONTROLLING LEAKAGE CURRENT IN AN INTEGRATED CIRCUIT	HOUSTON, THEODORE W.
09316881	6177300	150	05/21/1999	MEMORY WITH STORAGE CELLS HAVING SOI DRIVE AND ACCESS TRANSISTORS WITH TIED FLOATING BODY CONNECTIONS	HOUSTON, THEODORE W.
09321867	Not Issued	161	05/28/1999	SEMICONDUCTOR ON SILICON (SOI) TRANSISTOR WITH A HALO IMPLANT	HOUSTON, THEODORE W.
09330770	6261879	150	06/11/1999	DIFFERENTIAL SOI AMPLIFIERS HAVING TIED FLOATING BODY CONNECTIONS	HOUSTON, THEODORE W.
09335193	6074920	150	06/17/1999	SELF-ALIGNED IMPLANT UNDER TRANSISTOR GATE	HOUSTON, THEODORE W.
09346436	7153756	150	07/01/1999	BONDED SOI WITH BURIED INTERCONNECT TO HANDLE OR DEVICE WAFER	HOUSTON, THEODORE W.
09349626	Not Issued	161	07/08/1999	SELECTIVELY INCREASED INTERLEVEL CAPACITANCE	HOUSTON, THEODORE W.
09365068	6261886	150	07/30/1999	INCREASED GATE TO BODY COUPLING AND APPLICATION TO DRAM AND DYNAMIC CIRCUITS	HOUSTON, THEODORE W.
09368387	6548359	150	08/04/1999	ASYMMETRICAL DEVICES FOR SHORT GATE LENGTH PERFORMANCE WITH DISPOSABLE SIDEWALL	HOUSTON, THEODORE W.
09379667	6307281	150	08/24/1999	SYSTEM AND METHOD FOR REDUCING POWER	HOUSTON, THEODORE W.

				DISSIPATION IN A CIRCUIT	
09395027	6351176	150	09/13/1999	PULSING OF BODY VOLTAGE FOR IMPROVED MOS INTEGRATED CIRCUIT PERFORMANCE	HOUSTON, THEODORE W.
09422861	Not Issued	168	10/25/1999	SELF-ALIGNED IMPLANT UNDER TRANSISTOR GATE	HOUSTON, THEODORE W.
60008310	Not Issued	159	12/07/1995	INSTANT REPLAY SYSTEM	HOUSTON, THEODORE W.
60010927	Not Issued	159	01/31/1996	SELECTIVELY LIMITING CURRENT IN AN INTEGRATED CIRCUIT	HOUSTON, THEODORE W.
60010928	Not Issued	159	01/31/1996	OPTIMIZING THE OPERATING CHARACTERISTICS OF A CMOS INTEGRATED CIRCUIT	HOUSTON, THEODORE W.
60013364	Not Issued	159	03/13/1996	SEMICONDUCTOR ON SILICON (SOI) TRANSISTOR WITH A HALO IMPLANT	HOUSTON, THEODORE W.
60016369	Not Issued	159	04/19/1996	OPTIMIZING THE OPERATING CHARACTERISTICS OF A CMOS INTEGRATED CIRCUIT	HOUSTON, THEODORE W.
60018300	Not Issued	159	05/24/1996	SOI DRAM HAVING P-DOPED POLY GATE FOR A MEMORY PASS TRANSISTOR	HOUSTON, THEODORE W.
60028292	Not Issued	159	10/11/1996	ADAPTIVELY RECONFIGURABLE INTEGRATED CIRCUIT AND METHOD THEREFOR	HOUSTON, THEODORE W.
60031487	Not Issued	159	12/06/1996	BURIED OXIDE WITH A THERMAL EXPANSION MATCHING LAYER FOR SOI	HOUSTON, THEODORE W.
60044257	Not Issued	159	04/30/1997	INCREASED EFFECTIVE TRANSISTOR WIDTH USING DOUBLE SIDEWALL SPACERS	HOUSTON, THEODORE W.
60045115	Not Issued	159	04/30/1997	SELF-ALIGNED TRENCHED-CHANNEL LATERAL-CURRENT-FLOW TRANSISTOR	HOUSTON, THEODORE W.
60050979	Not Issued	159	06/20/1997	PROCESS FOR DEFINING ULTRA-THIN GEOMETRIES	HOUSTON, THEODORE W.

60057194	Not Issued	159	08/29/1997	STRUCTURE AND METHOD FOR A SELF-ALIGNED BACK GATE IN A SEMICONDUCTOR COMPONENT	HOUSTON, THEODORE W.
60057272	Not Issued	159	08/29/1997	SELF-ALIGNED IMPLANT UNDER TRANSISTOR GATE	HOUSTON, THEODORE W.
60060279	Not Issued	159	09/29/1997	FEEDBACK STAGE FOR PROTECTING A DYNAMIC NODE IN AN INTEGRATED CIRCUIT HAVING DYNAMIC LOGIC	HOUSTON, THEODORE W.

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60060348	Not Issued	159	09/29/1997	INTEGRATED CIRCUIT HAVING DYNAMIC LOGIC WITH REDUCED STANDBY LEAKAGE CURRENT	HOUSTON, THEODORE W.
60061128	Not Issued	159	10/06/1997	CIRCUIT HAVING DYNAMIC THRESHOLD VOLTAGE	HOUSTON, THEODORE W.
60068279	Not Issued	159	12/19/1997	SYSTEM AND METHOD FOR CONTROLLING LEAKAGE CURRENT IN AN INTEGRATED CIRCUIT	HOUSTON, THEODORE W.
60068303	Not Issued	159	12/19/1997	SYSTEM AND METHOD FOR CONTROLLING LEAKAGE CURRENT IN AN INTEGRATED CIRCUIT USING CURRENT LIMITING DEVICES	HOUSTON, THEODORE W.
60095254	Not Issued	159	08/04/1998	INCREASED GATE TO BODY COUPLING AND APPLICATION TO DRAM AND DYNAMIC CIRCUITS	HOUSTON, THEODORE W.
60095291	Not Issued	159	08/04/1998	SELECTIVELY INCREASED INTERLEVEL CAPACITANCE	HOUSTON, THEODORE W.
60095293	Not Issued	159	08/04/1998	BONDED SOI WITH BURIED INTERCONNECT TO HANDLE OR DEVICE WAFER	HOUSTON, THEODORE W.
60095327	Not Issued	159	08/04/1998	ASYMMETRICAL DEVICES FOR SHORT GATE LENGHT PERFORMANCE WITH DISPOSABLE SIDEWALL	HOUSTON, THEODORE W.
60099632	Not Issued	159	09/09/1998	SYSTEM AND METHOD FOR REDUCING POWER DISSIPATION IN A CIRCUIT	HOUSTON, THEODORE W.
60100202	Not	159	09/14/1998	PULSING OF BODY VOLTAGE	HOUSTON,

	Issued			FOR IMPROVED MOS INTEGRATED CIRCUIT PERFORMANCE	THEODORE W.
60105962	Not Issued	159	10/28/1998	LOCAL INTERCONNECT STRUCTURES AND METHODS	HOUSTON, THEODORE W.
60160495	Not Issued	159	10/20/1999	SEMICONDUCTOR DEVICE WITH FULLY SELF-ALIGNED LOCAL INTERCONNECTS, AND METHOD FOR FABRICATION THE DEVICE	HOUSTON, THEODORE W.
60161651	Not Issued	159	10/20/1999	SEMICONDUCTOR DEVICE WITH FULLY SELF-ALIGNED LOCAL INTERCONNECTS, AND METHOD FOR FABRICATING THE DEVICE	HOUSTON, THEODORE W.
60171727	Not Issued	159	12/22/1999	METHOD AND APPARATUS FOR REDUCING CROSS-TALK AND FACILITATING ENERGY STORAGE IN A HIGH-FREQUENCY INTEGRATED CIRCUIT	HOUSTON, THEODORE W.
60171729	Not Issued	159	12/22/1999	METHOD FOR CONTROLLING AN IMPLANT PROFILE IN THE CHANNEL OF A TRANSISTOR	HOUSTON, THEODORE W.
60171770	Not Issued	159	12/22/1999	INTEGRATED CIRCUIT WITH CLOSELY SPACED COMPONENTS, AND A METHOD OF MAKING IT	HOUSTON, THEODORE W.
60172889	Not Issued	159	12/21/1999	SILICON-ON-INSULATOR FORMATION USING AN UNDERLYING POROUS SILICON LAYER	HOUSTON, THEODORE W.
60172894	Not Issued	159	12/21/1999	NOVEL CONTACT/VIA FOR DECREASED CAPACITANCE AND GREATER ALIGNMENT TOLERANCE	HOUSTON, THEODORE W.
60259402	Not Issued	159	12/30/2000	Spimox/simox combination with itox option	HOUSTON, THEODORE W.
11445428	Not Issued	41	06/01/2006	8T SRAM cell with higher voltage on the read WL	HOUSTON, THEODORE WARREN
11511800	Not Issued	30	08/29/2006	Memory with low power mode for WRITE	HOUSTON, THEODORE WARREN

60874768	Not Issued	20	12/14/2006	Universal structure for SRAM cell characterization	HOUSTON, THEODORE WARREN

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